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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,249	02/22/2002	Kuo-Hwa Yu	PAT-1399	6372

7590 08/06/2004

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EXAMINER	
PARK, ILWOO	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 08/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/081,249	YU, KUO-HWA
	Examiner	Art Unit
	Ilwoo Park	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/24/2004 has been entered.

2. Claim 1 is amended and claims 5-6 are canceled. Jolley et al, Collins, Chen, and Chang et al were cited in the last office action. The following rejections now apply. Claims 1-4 and 17 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Jolley et al., US patent No. 5,832,244.

As to claim 1, Jolley et al teach a peripheral or memory device having a bus, and a bus switching circuit that comprises:

a first bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] signals in a first format;

a second bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] signals in a second format;

a first bus snoop circuit [col. 6, lines 34-37] coupled to the bus;

a second bus snoop circuit [col. 6, lines 34-37] coupled to the bus;

a switch coupled to the first bus snoop circuit for receiving a first bus detect signal [col. 10, lines 60-63] therefrom, and the switch coupled to the second bus snoop circuit for receiving a second bus detect signal [col. 10, lines 63-66] therefrom;

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, depending on the nature of the first and second detect signals; and

wherein the switch, the first bus snoop circuit and the second bus snoop circuit are separated from each other [functionally separated from each other in order to detect a plurality of different types of interface buses]

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jolley et al., US patent No. 5,832,244 in view of Collins, US patent No. 5,671,355.

As to claims 3 and 5, Jolley et al teach a peripheral or memory device comprising:

a bus [host bus 18, 24]; and

a bus switching circuit that comprises:

a first bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] signals in a first format;

a second bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] signals in a second format;

a switch for receiving a bus select signal [type of the host bus: col. 10, lines 60-66]; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, depending on the nature of the bus select signal.

However, Jolley et al teach do not disclose a micro-controller which generates a bus select signal selected by the micro-controller without receiving bus data from the bus.

Collins teaches a peripheral or memory device, for interfacing a plurality of different types of host bus, having a micro-controller [configuration configure means 15 without the network and bus type determination means 25 in col. 8, lines 19-31] which generates a bus select signal selected by the micro-controller without receiving bus data from the bus. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jolley et al and Collins because they both teach interfacing a plurality of different types of host bus and Collins' teaching of a micro-controller which generates a bus select signal selected by the micro-controller without receiving bus data from the bus would increase user friendliness in selecting a bus type by a user manually [Collins: col. 8, lines 19-31] and/or further increase reliability by eliminating uncertainty of detecting of a bus type using signal levels of selected bus pins [Jolley et al: col. 11, lines 8-12].

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jolley et al., US patent No. 5,832,244 in view of Chang et al., US patent No. 6,286,097.

As to claim 2, Chang et al teach a bus can be either [col. 2, lines 10-14; figs. 1-2] an ISA bus or an LPC bus and an ISA bus decoder circuit and an LPC bus decoder circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an ISA bus decoder circuit and an LPC bus decoder circuit into the plurality of Jolley et al's bus decoder circuits in

order to increase adaptability for a bus connection [Chang et al: col. 2, lines 10-14].

8. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jolley et al and Chen as applied to claims 3 and 5 above, and further in view of Chang et al., US patent No. 6,286,097.

As to claims 4 and 6, Chang et al teach a bus can be either [col. 2, lines 10-14; figs. 1-2] an ISA bus or an LPC bus and an ISA bus decoder circuit and an LPC bus decoder circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an ISA bus decoder circuit and an LPC bus decoder circuit into the plurality of Jolley et al and Collins' bus decoder circuits in order to increase adaptability for a bus connection [Chang et al: col. 2, lines 10-14].

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jolley et al., US patent No. 5,832,244 in view of Collins, US patent No. 5,671,355.

As to claim 17, Jolley et al do not disclose generating the bus detect signals based on a series of I/O writes.

Collins teach generating bus detect signals based on a series of I/O writes [signature signals of the bus: col. 7, lines 40-47]. Therefore, it would have been obvious to one of ordinary skill in the art of bus type identification at the time the invention was made to include generating bus detect signals based on a series of I/O writes in order to increase reliability by eliminating uncertainty of detecting of

a bus type using signal levels of selected bus pins [Jolley et al: col. 11, lines 8-12].

Response to Arguments

10. Applicant's arguments with respect to claims 1-2 filed 12/29/2003 have been fully considered but they are not persuasive. The examiner respectfully disagrees the applicant allegation of a) the switch, the first bus snoop circuit and the second bus snoop circuit of Jolly are separated from each other and b) Collins has no micro-controller which is included in the network and bus type determination means 25.

For the point a), though the applicant points the fig. 1 as a support of the added limitations in claim 1 describing that *the switch, the first bus snoop circuit and the second bus snoop circuit are separated from each other*, the fig. 1 merely shows the switch, the first bus snoop circuit and the second bus snoop circuit are figuratively drawn in separate blocks or boxes from each other not for actual functional circuitries having electronic components comprising ICs, resistors, capacitors, etc. but only for a schematic functional block diagram; the fig. 1 actually shows the switch, the first bus snoop circuit and the second bus snoop circuit are directly connected each other and can't be separable each other because all of the switch, the first bus snoop circuit and the second bus snoop circuit are commonly connected to bus 30.

For the point b), Collins has a micro-controller [configuration configure means 15] which works without the network and bus type determination means 25.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (703) 308-7811. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Hand-delivered responses should be brought to US Patent and Trademark Office, 2011 South Clark Place, Customer Window, Crystal Plaza Two, Lobby, Room 1B03, Arlington, VA 22202.

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park
Primary Examiner
August 2, 2004